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| EXAMINER | |
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| LI, AIMEE J | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/704,467 | ROTH ET AL. | |
| | Examiner | Art Unit | |
| | Aimee J. Li | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3,5-9,11-16,18-21 and 23-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,3,5-8,24,25,30 and 31* is/are allowed.

6)☒ Claim(s) *9,13-16,19-21 and 26-29* is/are rejected.

7)☒ Claim(s) *11,12,18 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1, 3, 5-9, 11-16, 18-21, and 23-31 have been considered.

### *Papers Submitted*

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 01 June 2007.

### *Allowable Subject Matter*

3. Claims 1, 3, 5, 6, 7, 8, 24, 25, 30, and 31 are allowed.

4. Claims 11, 12, 18, and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: The allowable claims contain the limitations, taking claim 11 as exemplary, "determining a validity of each of the plurality of instructions before processing by reading bits in each instruction indicating a width of the instruction." The limitation was found in the prior art searched, specifically determining the validity of an instruction of each of the plurality of instructions before processing, but did not suggest or provide a sound motivation for combining, since most test interfaces are developed under the assumption that they will be written to be automatically compatible with the system.

### *Claim Rejections - 35 USC § 102*

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 9, 16, 21, and 27-29 are rejected under 35 U.S.C. 102(e) as being taught by Xu et al., U.S. Patent Number 6,070,252 (herein referred to as Xu).

8. Referring to claim 9, Xu has taught a method of providing instructions to a processor, the method comprising:

a. Loading a plurality of instructions into an emulation instruction register from a test interface (Xu Abstract; column 3, lines 32-62; column 4, line 32 to column 5, line 2' column 5, lines 25-56; column 6, lines 4-63; Figure 1A; Figure 1B; Figure 3; and Figure 4). In regards to Xu, the emulation instruction register can be any number of registers that accept the instructions indicated by the test interface, including the instruction register 308 in Figure 3.

b. Receiving a run-test idle state signal, the run-test idle state signal indicating entry of the test interface into a run-test idle state (Xu Abstract; column 3, lines 32-62; column 4, line 32 to column 5, line 2' column 5, lines 25-56; column 6, lines 4-63; Figure 1A; Figure 1B; Figure 3; and Figure 4);

c. Providing the plurality of instructions to the processor in response to the receipt of the run-test idle state signal (Xu Abstract; column 3, lines 32-62; column 4, line 32 to column 5, line 2' column 5, lines 25-56; column 6, lines 4-63; Figure 1A; Figure 1B; Figure 3; and Figure 4); and

d. Processing the plurality of instructions without receiving another run-test idle state signal (Xu Abstract; column 3, lines 32-62; column 4, line 32 to column 5,

line 2' column 5, lines 25-56; column 6, lines 4-63; Figure 1A; Figure 1B; Figure 3; and Figure 4). In regards to Xu, the initial instruction to set the DFU flags is issued in response to the run-test idle state signal, and these flags are used to determine where the instructions and data for the test routine are provided from.

9. Referring to claim 16, Xu has taught a processor comprising:

a. A test interface (Xu Abstract; column 3, lines 32-62; column 4, line 32 to column 5, line 2; column 5, lines 25-56; column 6, lines 4-63; Figure 1A; Figure 1B; Figure 3; and Figure 4);

b. An emulation instruction register adapted to store a plurality of emulation instructions received from the test interface (Xu Abstract; column 3, lines 32-62; column 4, line 32 to column 5, line 2; column 5, lines 25-56; column 6, lines 4-63; Figure 1A; Figure 1B; Figure 3; and Figure 4). In regards to Xu, the emulation instruction register can be any number of registers that accept the instructions indicated by the test interface, including the instruction register 308 in Figure 3.

c. Emulation control logic adapted to supply the plurality of emulation instructions to a processor pipeline in response to detection of an entry of the test interface into a run-test idle state (Xu Abstract; column 3, lines 32-62; column 4, line 32 to column 5, line 2; column 5, lines 25-56; column 6, lines 4-63; Figure 1A; Figure 1B; Figure 3; and Figure 4). In regards to Xu, the initial instruction to set the DFU flags is issued in response to the run-test idle state signal, and these flags are

used to determine where the instructions and data for the test routine are provided from.

d. A decoder to receive the plurality of instructions for processing (Xu Abstract; column 3, lines 32-62; column 4, line 32 to column 5, line 2; column 5, lines 25-56; column 6, lines 4-63; column 6, line65 to column 7, line 15; Figure 1A; Figure 1B; Figure 3; Figure 4; and Figure 5). In regards to Xu, the processor core is shown in relation to the system pin approach described, however, the essential elements in the processing core, e.g. Instruction Fetch Unit, Instruction Decoder, Pipeline Sequencer, Execution units, and Register File, remain the same. The only difference between the processor core in Figure 5 and the CPU core in Figure 4 would be the BOSTPAT and DATA-VALID pins (Xu column 7, lines 28-31).

10. Referring to claim 21, Xu has taught an apparatus, including operating instructions residing on a machine-readable storage medium, for use in a device to handle a plurality of emulation instructions, the operating instructions causing the device to:

a. Load the plurality of emulation instructions into a single emulation instruction register (Xu Abstract; column 3, lines 32-62; column 4, line 32 to column 5, line 2; column 5, lines 25-56; column 6, lines 4-63; Figure 1A; Figure 1B; Figure 3; and Figure 4). In regards to Xu, the emulation instruction register can be any number of registers that accept the instructions indicated by the test interface, including the instruction register 308 in Figure 3.

b. Have a test interface enter a run-test idle state (Xu Abstract; column 3, lines 32-62; column 4, line 32 to column 5, line 2; column 5, lines 25-56; column 6, lines 4-63; Figure 1A; Figure 1B; Figure 3; and Figure 4);

c. Provide the plurality of emulation instructions to a processor in response to entry of the test interface into the run-test idle state (Xu Abstract; column 3, lines 32-62; column 4, line 32 to column 5, line 2; column 5, lines 25-56; column 6, lines 4-63; Figure 1A; Figure 1B; Figure 3; and Figure 4); and

d. Process the plurality of emulation instructions (Xu Abstract; column 3, lines 32-62; column 4, line 32 to column 5, line 2; column 5, lines 25-56; column 6, lines 4-63; Figure 1A; Figure 1B; Figure 3; and Figure 4). In regards to Xu, the initial instruction to set the DFU flags is issued in response to the run-test idle state signal, and these flags are used to determine where the instructions and data for the test routine are provided from.

11. Referring to claim 27, Xu has taught the processor of Claim 16, wherein the emulation control logic comprises a state machine (Xu Abstract; column 3, lines 32-62; column 4, line 32 to column 5, line 2; column 5, lines 25-56; column 6, lines 4-63; Figure 1A; Figure 1B; Figure 3; and Figure 4).

12. Referring to claim 28, Xu has taught the processor of Claim 16 further comprises a multiplexer to select between an instruction for the plurality of instructions to send to the processor pipeline (Xu Abstract; column 3, lines 32-62; column 4, line 32 to column 5, line 2; column 5, lines 25-56; column 6, lines 4-63; Figure 1A; Figure 1B; Figure 3; and Figure 4).

13. Referring to claim 29, Xu has taught the apparatus of Claim 21, further comprising an in-circuit emulator to monitor operations of the processor (Xu Abstract; column 3, lines 32-62; column 4, line 32 to column 5, line 2; column 5, lines 25-56; column 6, lines 4-63; Figure 1A; Figure 1B; Figure 3; and Figure 4). In regards to Xu, the BIST monitors whether a circuit is performing correctly, since it tests itself to ensure proper functionality.

***Claim Rejections - 35 USC § 103***

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 13-15, 19, 20, and 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Xu et al., U.S. Patent Number 6,070,252 (herein referred to as Xu), as applied to claims 9, 16, and 21 above, in view of Nakano, U.S. Patent Number 5,774,737 (herein referred to as Nakano). Xu has not taught

a. Loading a next instruction into the emulation instruction register if a no-operation instruction is loaded (Applicant's claims 13 and 19).

b. Providing the plurality of instructions to the processor a plurality of times without reloading the instruction register (Applicant's claim 14).

c. Providing the plurality of instructions to a digital signal processor (Applicant's claims 15 and 20).

d. Wherein the emulation instruction register comprises first and second registers (Applicant's claim 26).

16. Nakano has taught

a. Loading a next instruction into the emulation instruction register if a no-operation instruction is loaded (Applicant's claims 13 and 19) (Nakano column 2, lines 37-40 and 63-65; column 9, lines 11-23; column 10, line 57 to column 11, line2; Figure 2; and Figure 5).

b. Providing the plurality of instructions to the processor a plurality of times without reloading the instruction register (Applicant's claim 14) (Nakano column 2, lines 37-40 and 63-65; column 9, lines 11-23; column 10, line 57 to column 11, line2; Figure 2; and Figure 5).

c. Providing the plurality of instructions to a digital signal processor (Applicant's claims 15 and 20) (Nakano column 5, line 44 to column 6, line 3 and Figure 1).

d. Wherein the emulation instruction register comprises first and second registers (Applicant's claim 26) (Nakano column 5, lines 25-29; column 6, lines 4-25; Figure 1; and Figure 2).

17. A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Nakano, that the VLIW system uses instruction memories more effectively, executes more instructions simultaneously, and has compatible with programs for conventional processors (Nakano column 1, line 63 to column 2, lines 11). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the VLIW system of Nakano in the device of Xu to improve memory usage, instruction execution, and compatibility.

***Response to Arguments***

18. Examiner withdraws the rejection of claims 1, 3, 5, 6, 7, 8, 24, 25, 30, and 31 under 35 U.S.C. 101 in favor of Applicants' arguments.

19. Applicants' argues in essence on pages 10-17

> ...Xu neither describes nor suggests that a plurality of instructions that has been provided to a processor in response to receipt of a run-test idle state signal is processed without receiving another run-test idle state signal...

20. This has not been found persuasive. As described in the previous rejection, which is copied above, Xu issues an initial instruction to set the DFU flags in response to the run-test idle state signal and the flags determine where the rest of the routine is provided from, i.e. where the rest of the instructions are retrieved from. As Xu describes in column 3, lines 32-62 test control logic receives and executes a first instruction that sets the flags. The flags then help the system determine where the rest of the test routine and data are provided from. The signal signifying the first instruction is only sent once to the test control and then the rest of the test routine, i.e. multiple instructions in the test routine, are fetched by the test control logic.

***Conclusion***

21. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

22. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aimee J Li
Examiner
Art Unit 2183

17 August 2007

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100